FET

A 600 V SiC Trench JFET
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2 kV 4H-SiC Junction FETs
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A Novel High-Voltage Normally-Off 4H-SiC Vertical JFET
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Large Area (3.3mm**33.3mm) Power MOSFETs in 4H-SiC**
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4H-SiC Delta-Doped Accumulation-Channel MOS-FET (DACFET)
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Matsushita Electric Industrial Co., Ltd., Japan

5.0 kV 4H-SiC SEMOSFET with Low RonS of 88 mW **Wcm 2**
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High Performance UMOSFETs on 4H-SiC
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SiC vertical DACFET (Delta-Doped Accumlation Channel MOSFET)
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Silicon/Oxide/Silicon Carbide (SOSiC)—a New Approach for High Voltage, High Frequencies Integrated Circuits
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A 600V SiC Trench JFET

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Abstract: 4H silicon carbide trench vertical JFET has been fabricated with a blocking voltage of 600V and specific on-resistance of 5mΩ-cm^2. 2A FETs with an average on-voltage of 1Vand 40% yield have been demonstrated. To our knowledge this is the lowest specific on-resistance for a 600V FET reported. Devices with similar voltage ratings reported in the past showed much higher specific on-resistance. For instance, 40mΩ-cm^2 for 700V, expected based on simulations for ACCUFET, by Motorola [1], 18mΩ-cm^2 for 600V VJFET, by Siemens [2], 18 mΩ-cm^2 for the best device, breakdown voltage 350-450V, by North Carolina State University. From a website [4] of the SiC research group at purdue, (updated Jan 20 2001), the lowest on-resistance reported by any group, is over 10mΩ-cm^2.

The structure of the device is shown in fig. 1.This trench JFET has 4μm deep trenches, with trench bottom implanted with p-type dopants and trenches filled with polysilicon to form the gate. The P$^+$ at the trench bottom serves to protect the trench corners from high electric fields, it is connected to the gate to make the device a JFET. Starting from an n/N$^+$ epi, with the epitaxial layer doped 1e16cm^{-3}, 10um thick, trenches using Ni mask, in an SF_6 chemistry based RIE process developed at the Rockwell Science Center. The oxide isolating the gate from the trench sidewalls is deposited by LTO and subsequently re-oxidized at 1150C. LPCVD deposition of polysilicon is then performed to fill the trenches. The polysilicon is then RIE etched to remove excess polysilicon on the source mesas. Fig. 2 Shows an SEM picture of the device after the polysilicon etching. Following the polysilicon planarization, contacts are defined and metal deposited. To simplify the process, the contacts were not sintered. In the following lots we plan to alloy the contacts to reduce the contact resistance.

Fig. 3 shows the family of drain current vs. drain voltage characteristic of the FET for various gate voltages. This is a normally on FET, and requires negative voltage to turn-off. It is possible to use this device under 'normally –off' conditions by use of a low voltage silicon MOSFET in series, in a cascode configuration, as described in [2]. Fig. 4 shows the blocking characteristics of the FET. It can be seen that the device blocking voltage is over 600V. However in order for the device to block 600V, -30V on the gate is needed. A plot of the blocking voltages vs. device position on the wafer is shown in Fig. 5 for the –20V gate bias. With –20V on the gate the working devices could block between 400-500V. Shown in Fig. 6 is the on-voltage vs. device position for the FET, at a drain current of 1A. It can be seen that over 90% of the devices have on-voltages between 0.4 and 0.6 v.

We will report the results of the FET with improved contacts in the paper. Further we will also describe the device design and process issues for this device. High temperature will also be presented in the paper.

Refrences

1. Wang, Y.; Weitzel, C.; and Bhatnagar, M., "Accumulation-mode SiC power MOSFET design issues" ICSRM '99, pg 1287-90.
2. Mitlehner, H. et al, "Dynamic characteristics of High voltage 4H-SiC vertical JFETs", ISPSD '99, pg. 339-42.
3. Chilukuri, R.K.; Shenoy, P.M.; and Baliga, B.J., "High-temperature operation of SiC planar ACCUFET", IEEE trans. Industry Applications, Nov.-Dec. '99, vol. 35, no. 6., pg 1458-62.
4. Purdue Wide Band Gap Research, updated Jan 20 2001. Figure 2.

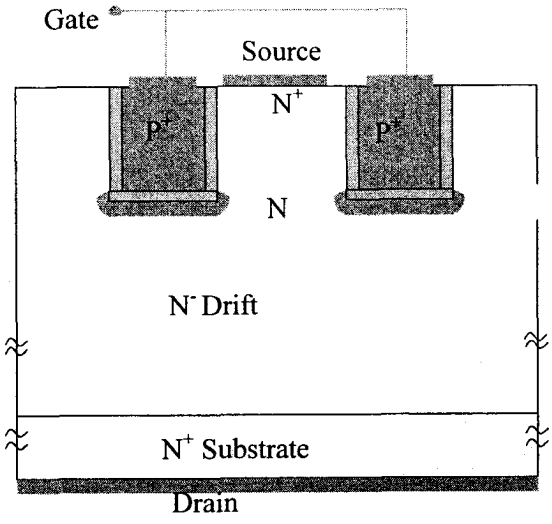

Fig.1 Cross-section of the device

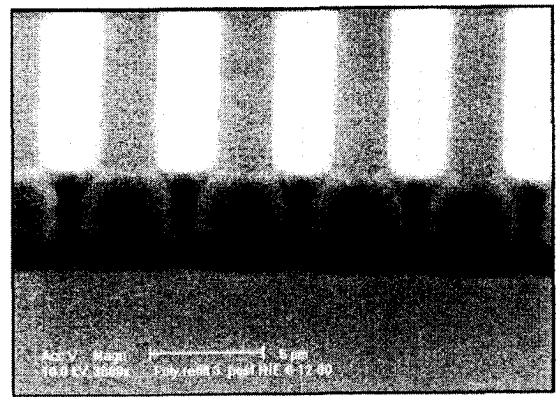

Fig.2 SEM Picture of the device after polysilicon planarization

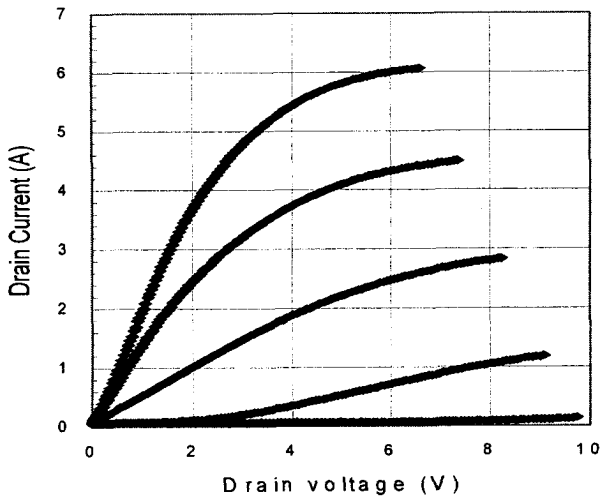

Fig. 3 Family of curves, Drain current vs. Drain voltage, Vg=0, -2, -4, -6, -8

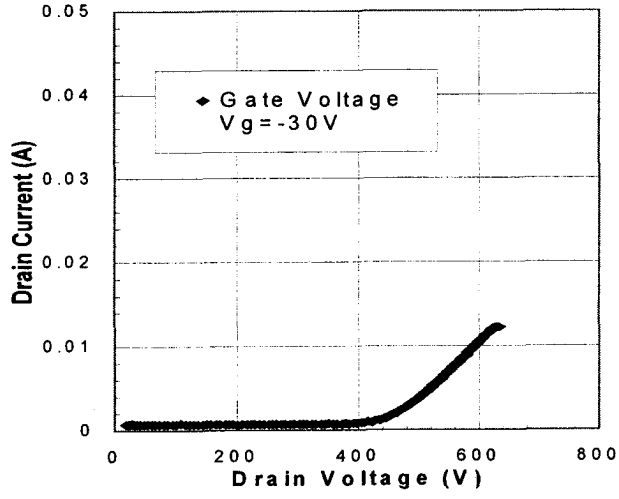

Fig. 4 Blocking characteristics of the FET. Vgs=-30V.

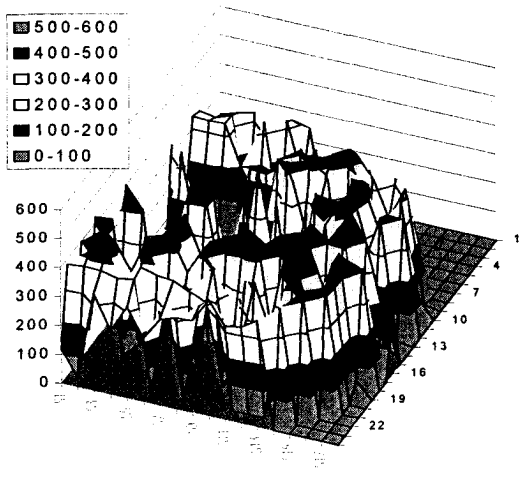

Fig. 5 Map of blocking voltage vs. device position for Vgs=-20V.

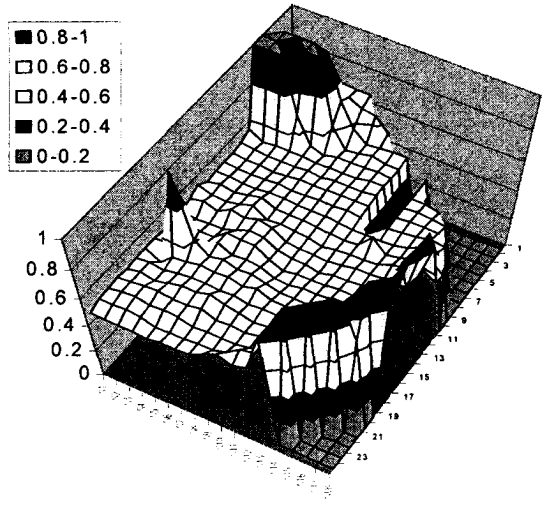

Fig. 6 Map of on-voltage vs. device position for Vgs=0V, at a current of 1A.

2 kV 4H-SiC Junction FETs

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The silicon carbide (SiC) SIT (static induction transistor) or Junction FET (JFET) will is expected to be appropriate for SiC devices because of no oxide-semiconductor interface in the channel [1]. A JFET with a novel gate structure, which can realize both low on-resistance and high blocking voltage, is proposed and demonstrated [2,3]. However, careful consideration of gate structures must be needed for reduce on-resistance. In this paper, vertical channel type 2 kV JFETs can successfully demonstrated and the effect of gate structure is also discussed.

Figure 1 shows schematic structures of fabricated JFETs. The doping level of n^- epitaxial layer is $2.5x10^{15}cm^{-3}$ and the thickness is 20 μm. In order to fabricate deep p gate and narrow channel, high energy multiple Al^+ implantation (730 keV and 870 keV) is used. Total dose of the p gate and the channel width are parameters for consideration. The n^+ source and p^+ gate contact are formed by N^+ and Al^+ implantation, respectively. After implantation, annealing at 1650 °C in argon is followed. Ni for the source electrode and Ti/Al for the gate electrode are evaporated and sintered. Figure 2 shows a top view of the fabricated source and gate electrodes. Figure 3 shows an example of measured drain I-V characteristics. Figure 4 shows a blocking property of a fabricated JFET, which indicates higher blocking capability than 2 kV. Figure 5 shows dependence of drain I-V curves on the channel width and the p gate dose measured at zero gate voltage. It can be found that on-resistance of high dose case ($2.9x10^{14}$ cm^{-2}) is higher than that of low dose case ($1.5x10^{13}$ cm^{-2}) shown in figure 6 as expected. Since the channel width dependence is not so strong, the low dose case is appropriate for fabrication. However, difference of on-resistance at 2 μm channel width is larger than expected value which is estimated by the simple model of depletion layer expansion. Two-dimensional effect is thought to be a reason of such large difference.

As a conclusion, vertical channel type JFETs are fabricated and higher blocking capability than 2 kV are demonstrated. The effect of gate structure is studied and it is found that low dose of the p gate is appropriate for the performance and fabrication process.

This work was performed under the management of FED as a part of the METI Program (R&D of Ultra-Low Loss Power Device Technologies) supported by NEDO.

References

[1] J. Nishizawa, et al., IEEE Trans. on Electron Devices, ED-22, pp. 185-197, 1975
[2] T. Iwasaki, et al., *Proc. ICSCRM95*, pp. 1085-1088, 1995
[3] H. Onose, at al., *Ext. Abst. UPD2000*, pp. 211-212, 2000

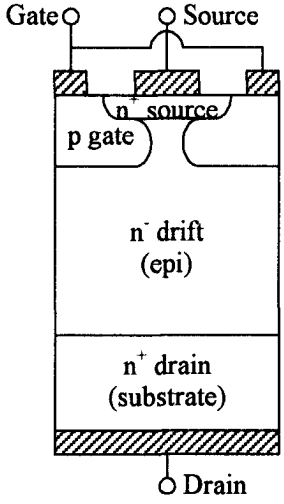

Fig.1 Schematic structure of a JFET

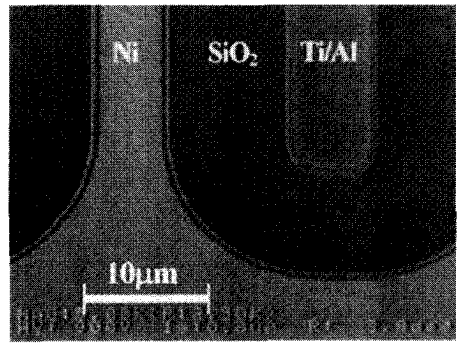

Fig.2 Top view a fabricated JFET.

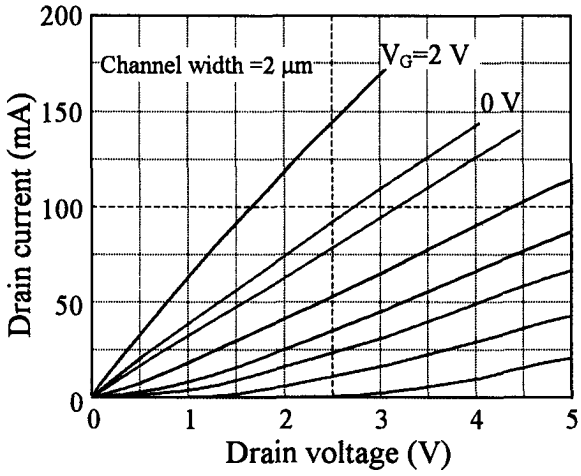

Fig.3 Gate voltage dependence of drain I-V characteristics

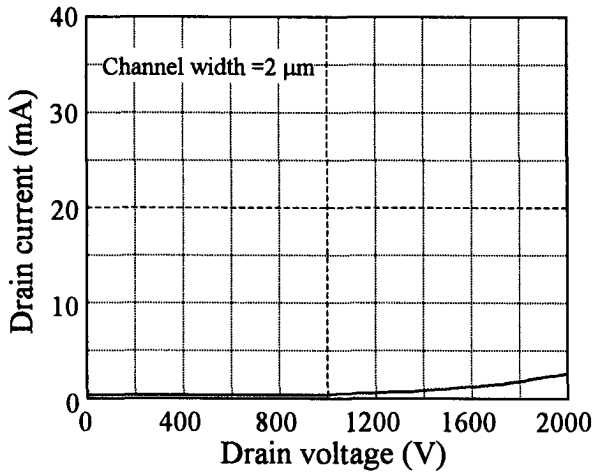

Fig.4 Broking characteristics

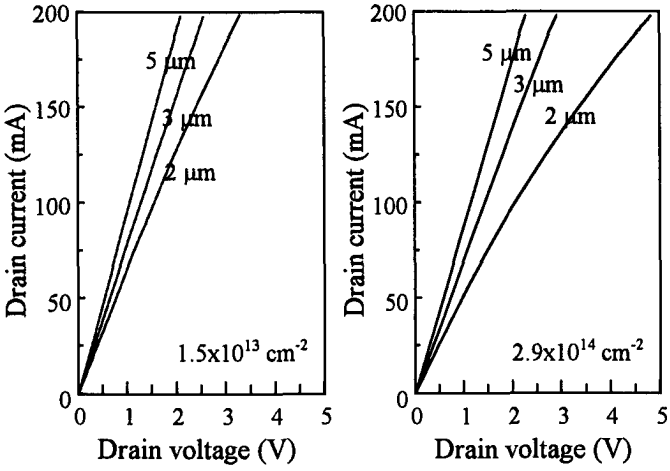

Fig.5 Dependence of drain I-V characteristics on channel width and p gate dose

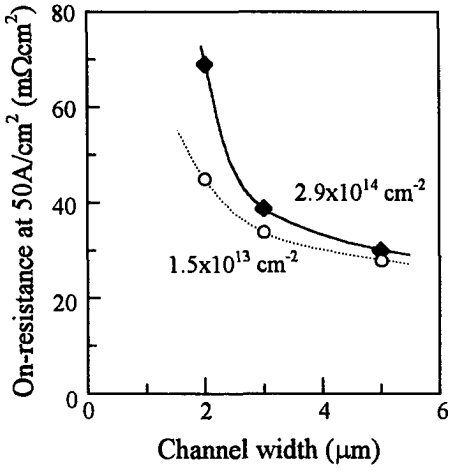

Fig.6 On-resistance versus channel width

A Novel High-Voltage Normally-Off 4H-SiC Vertical JFET

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The commercial availability of 3-inch wafers of 4H-SiC and the continuing effort in scaling up SiC substrates by a number of companies are creating the basis for an emerging SiC power electronic industry. Many 4H-SiC high voltage and high-speed devices have been demonstrated with the majority of them focusing on replicating the corresponding Si power devices in the hope of achieving higher power levels. It was pointed out in 1995 [1] that the reliability of gate oxide (SiO_2) in SiC power switches under both high temperature and high electric field is an intrinsic problem and gate-oxide free devices should be pursued. While many encouraging results have been reported over the years concerning the low inversion layer carrier mobility and different gate insulator reliability in 4H-SiC power switches a final solution suitable for practical applications may require a lot more research and investments. It is, therefore, desirable to develop SiC power switches free of gate oxide/insulator to take the full advantages of SiC material properties for high temperature power electronic applications. This work is focused on the development of a novel 4H-SiC unipolar power switch free of gate oxide/insulator.

Fig.1 shows the cross sectional view of a novel high voltage normally off vertical JFET (patent pending) in 4H-SiC based on MeV ion implantation technology. A buried P layer formed with MeV Al or Al plus C co-implantation is used to create the blocking junction and the horizontal channel. The semi-insulating layer formed by deep Vanadium implantation is used to terminate the horizontal channel so as to prevent the current conduction through the parasitic vertical PNP structure. The DC and transient characteristics of this switch are studied by way of two-dimensional numerical simulations with ISE-TCAD software. Fig.2 shows J-V curves of the device. It can be seen that the switch has a blocking voltage of 1644V at 300K and over 1,800V at 600K. The switch is normally-off and can be turned on to handle a high current density with gate voltages up to 2.75V and 2.06V at 300K and 600K, respectively, with a negligible gate current. The key design parameters for this device are vertical channel opening d and horizontal channel opening h. The optimized value for d is around 2.5μm as illustrated in Fig.3. It can be seen from Fig.4 that h=0.17μm can be used which

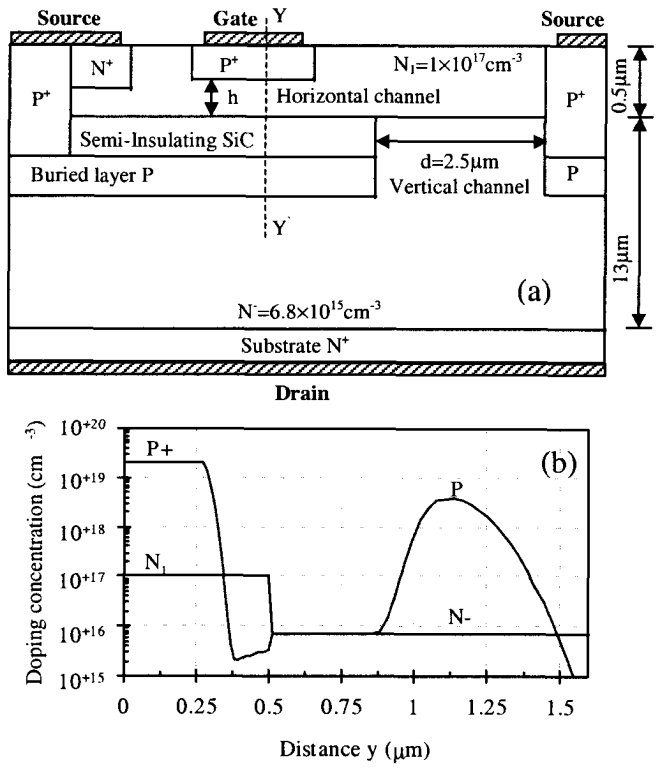

Fig.1 Normally-Off VJFET. (a) Cross sectional view. (b) Doping concentrations along the straight line YY'.

corresponds to a high J_F of 600A/cm^2 at a V_{Drain} of 3V. This unipolar switch has a very high switching speed. The results of transient simulations are presented in Fig.5 where the turn-on time of 211.5ns and the turn-off time of 144.7ns are basically limited by the applied dV_G/dt gating rate of 1.1×10^7V/s. With a drift layer doped mid-10^{15}cm^{-3}, a fully implanted planar 4H-SiC VJFET capable of blocking 1,790V has been demonstrated and the results will be presented.

Reference: [1]. J. H. Zhao, et al., "SiC UMOS and thyristor-based power switches", Proc. of 1st Workshop on HTPE for Vehicles, pp.36-43, 1995, Eaton Town, NJ.

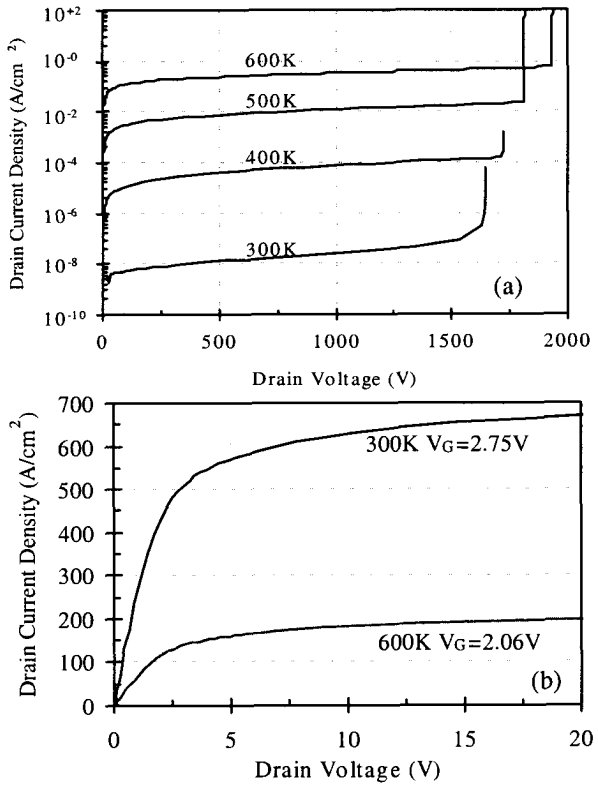

Fig.2 J_D-V_D curves at (a) off-state and (b) on-state.

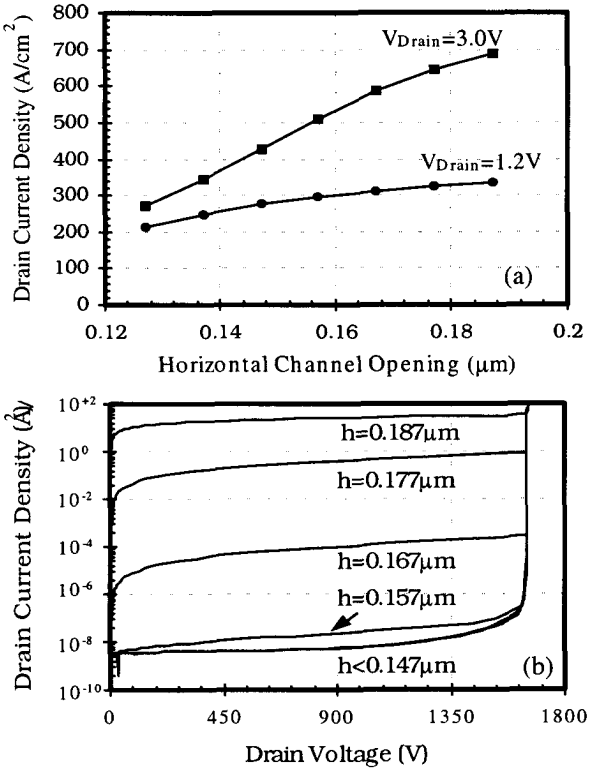

Fig.4. J_D-V_D curves with different horizontal channel opening h at 300K at (a) on-state and (b) off-state.

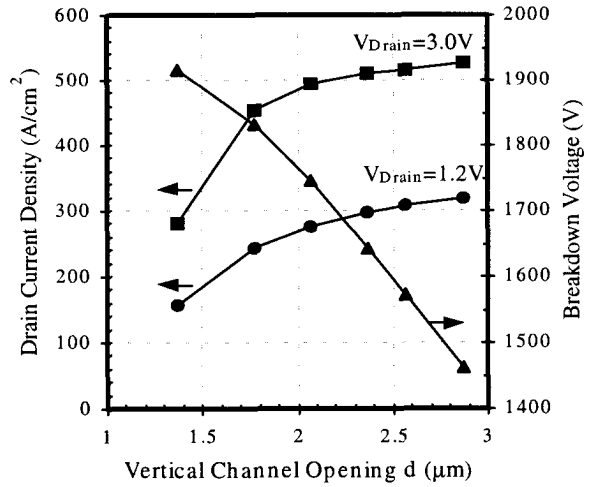

Fig.3 The effect of the vertical channel opening d at 300K.

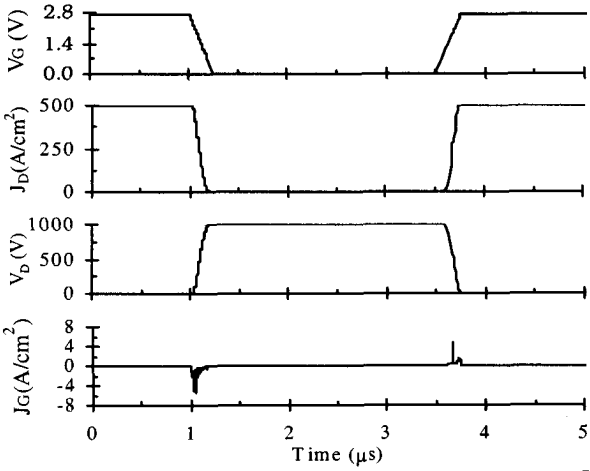

Fig.5 The switching waveforms with $dV_G/dt=1.1\times10^7$V/s at 300K.

Large Area (3.3mm x 3.3mm) Power MOSFETs in 4H-SiC

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This paper describes the design and fabrication of 4H-SiC Power MOSFETs. We have achieved 350 V, 10 A (V_F = 4.4 V) devices with an active area of 0.105 cm^2 (3.3 mm x 3.3 mm) which represents a specific on-resistance ($R_{on,sp}$) of 44 mΩ•cm^2. This has been made possible by using a buried channel device, resulting in a peak channel electron mobility of 195 cm^2/V•s. The previous results have been limited to less than 0.5 A in small area devices [1,2].

Figure 1 shows a schematic cross-section of the basic cell. A 25 μm thick, $2x10^{15}$ cm^{-3} doped n- type drift layer was grown on n+ 4H-SiC substrate. The cell pitch is 25 μm. The p-wells, JTE regions and the p^+ contacts are formed by aluminum implantation. The n^+ source regions are implanted with nitrogen. A buried n-type layer is created in the channel region with a charge of approximately $1.7x10^{12}$ cm^{-2}. All the implants are activated at 1600°C in Ar. The gate oxide is thermally grown in dry O_2 at 1200°C for 1 hr, followed by an anneal in at 1200°C Ar for 1 hr, followed by a re-oxidation anneal in wet O_2 at 950°C for 3 hrs. The gate metal consists of 0.5 μm thick sputtered Moly. The contacts to source, drain and p^+ regions are formed with 0.1 μm thick sintered Ni. Then, an inter-metal dielectric is deposited and via holes are opened. The final metal is a 2 μm thick Ti/Pt/Au layer.

The effective channel mobility measured on a 100 μm / 100 μm FATFET is shown in Figure 2. With zero bias to the p-well, the device is normally-on with a threshold voltage (V_{TH}) of -2 V and a very high peak effective channel mobility of 195 cm^2/V•s. This indicates the presence of a neutral n-type buried layer. At higher gate bias, the effect of the neutral n-type layer diminishes and all the curves come together to the surface electron mobility (~ 25 cm^2/V•s at V_{GS} = 20 V). The V_{TH} shifts positive as the charge in the n-type buried layer is reduced by applying negative biases on the p-well. This clearly shows that the devices can be made to be normally-off by reducing the n-type charge in the buried channel.

The on-state I-V characteristics of a 3.3x3.3 mm^2 4H-SiC Power MOSFET are shown in Figure 3. An I_D of 10 A was measured at a 4.4 V forward drop. This device is normally-on with a V_{TH} of -2 V, due to the relatively high dose of n-type charge in the p-well. A $R_{on,sp}$ value of 44 mΩ•cm^2 is obtained for the large 3.3x3.3 mm^2 device at a relatively low gate bias of 2.5 V. The breakdown voltage for the large device is only 350 V and a high leakage current is observed (Figure 4). Figures 5 and 6 show on-state and off-state I-V characteristics of a smaller 0.75x0.75 mm^2 device with a cell pitch of 16 μm. The device showed a reduced $R_{on,sp}$ value of 23 mΩ•cm^2 due to the smaller cell pitch, which resulted in smaller JFET resistance, and was able to block 1620V (V_g = -19V).

Recently, NO annealing of the gate oxide was shown to be very effective in improving effective channel mobility in 4H-SiC MOSFETs [3]. Figure 7 shows IV characteristics of a NO annealed (performed at Auburn Univ.) 4H-SiC power MOSFET (0.75x0.75 mm^2) without any buried channel charge. The device showed a $R_{on,sp}$ of 55 mΩ•cm^2 and a breakdown voltage of 1950 V (Figure 8). These devices are normally-off. The shape of the breakdown characteristics suggests open base bipolar breakdown, due to the high resistance of the p-well regions.

Acknowledgements: This work was supported by DARPA (Dr. D. Radack) and monitored by Dr. G. Campisi of ONR under the contract # N00014-99-C-0377.

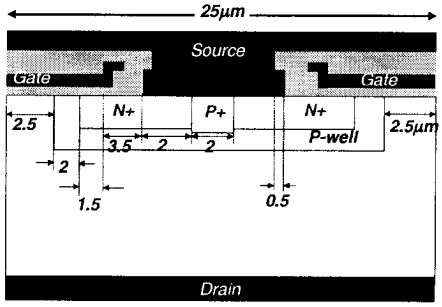

Figure 1. A schematic cross-section of the power MOSFET cell.

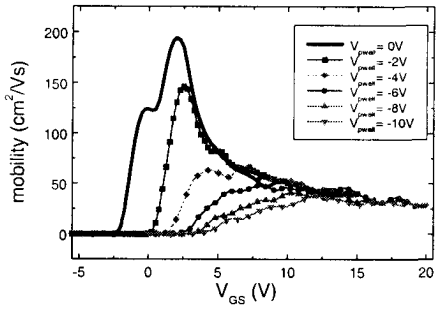

Figure 2. Effective channel mobility in a FATFET as a function of the gate bias and the back bias on the p-well.

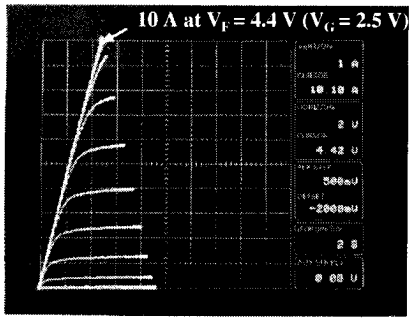

Figure 3. Forward I-V characteristics of a 3.3x3.3 mm^2 power MOSFET.

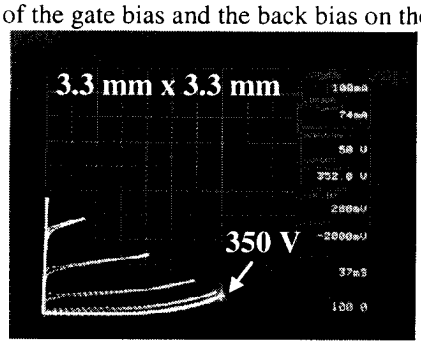

Figure 4. Blocking characteristics of the 3.3x3.3 mm^2 power MOSFET.

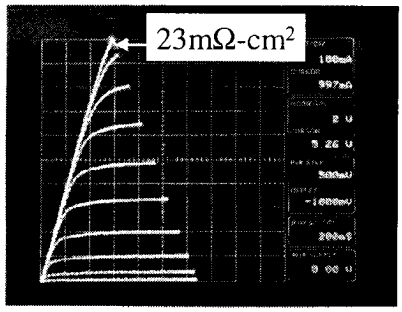

Figure 5. Forward I-V characteristics of a 0.75x0.75 mm^2 power MOSFET.

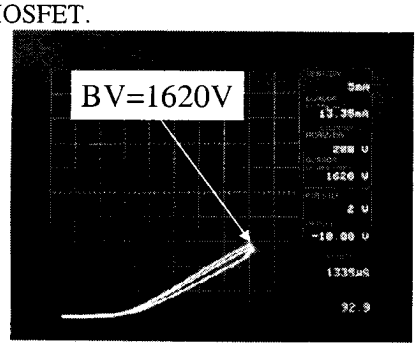

Figure 6. Blocking characteristics of the 0.75x0.75 mm^2 power MOSFET.

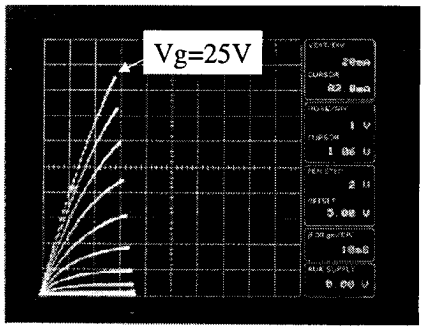

Figure 7. Forward I-V characteristics of NO annealed (courtesy of Prof. J. R. Williams) 4H-SiC power MOSFET (0.75x0.75mm^2).

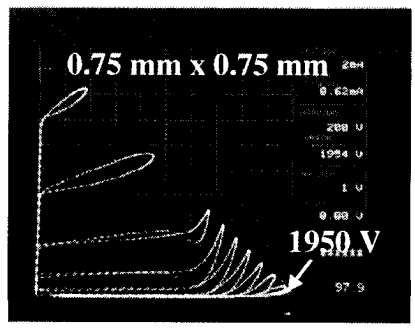

Figure 8. Blocking characteristics of the device shown in Figure 7. The device did not receive any buried channel charge.

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4H-SiC DELTA-DOPED ACCUMULATION-CHANNEL MOS FET

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We report on electronic properties of nitrogen-delta-doped SiC and propose its application for MOS-FET. Delta-doping distributions with high peak concentrations and narrow distribution widths were advantageous for a high Hall mobility. 4H-SiC delta-doped accumulation-channel MOS field effect transistors (DACFET) have been successfully fabricated. Delta-doping in CVD was performed by a pulse doping method using a pulse valve.[1] The valve can open and close within very short period less than 10 μs. The nitrogen gas as n-type dopant was injected into the reactor through the pulse valve. The delta-doped structure was confirmed by the C-V profiling technique. The doping distribution profile of the delta-doped SiC had strikingly narrow full width of half maximum (FWHM) of 10 nm, as shown in Fig.1. The peak concentration was as high as 10^{18} cm^{-3}. By Hall-effect of the delta-doped SiC, the temperature dependence of a Hall mobility and a carrier concentration was investigated. The Hall mobility enhancement was observed for the delta-doped structure over the corresponding uniformly doped SiC. The enhancement factor of 3 was obtained for the delta-doped SiC. The self-consistent calculation by the coupled sets of Poisson and Schrödinger equation suggests that the high mobility is related to the extension of the electron wave-function of the delta-doped layer to high purity SiC layers. The high mobility attracts considerable interest in MOS-FET having the delta-doped accumulation channel. Delta-doped accumulation-channel MOS-FET was fabricated. All epitaxial growth was carried out in the CVD on 4H-SiC (0001) off substrates. The device structure consisted of a 5 μm p-type SiC layer (9×10^{15} cm^{-3}), and an accumulation-channel layer consisting of a 10 nm delta-doped n^+-SiC layer and a 50 nm undoped SiC layer, as shown in Fig.2. The number of the delta-doped layers was five. N^+-source and drain regions were formed utilizing a multiple nitrogen implant profile at 30, 60, 100, 110, 130, 180, and 240 keV with doses of 5, 6, 8, 5, 10, 15, and 10 $\times10^{13}$ cm^{-2}, respectively. The implantation was carried out at 500 ℃. Implants were activated at 1500 ℃ for 30 min in an argon ambient. After standard RCA cleaning, the gate oxides (40 nm) was thermally grown using wet oxidation at 1100 ℃. The device was normally off and had a threshold voltage of 4.2 V although these gate-control properties depended on the delta-doped channel structure. The effective channel mobility derived from the I-V characteristics that was measured at low drain voltage of 0.5 V was higher than about 55 cm^2/Vs. The channel mobility increases with decreasing the gate voltage because of the reduction of the surface scattering. The excellent channel mobility of 113 cm^2/Vs was obtained at the gate voltage of 5 V, as shown in Fig.3. The device also had high drain current of up to 220 mA/mm at the drain voltage of 15 V.

Reference

[1] T. Yokogawa et al. J. Appl. Phys. 89, 1794 (2001).

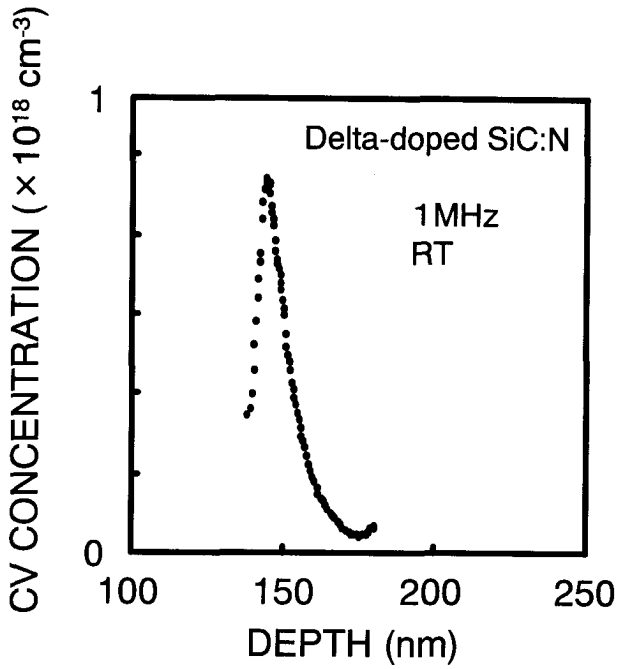

Fig.1. Room temperature capacitance-voltage profile for a delta-doped structure with nitrogen.

Nitrogen-delta-doped accumulation-channel
(5 periods : 10 nm delta-doped n⁺-SiC/ 50 nm undoped SiC)

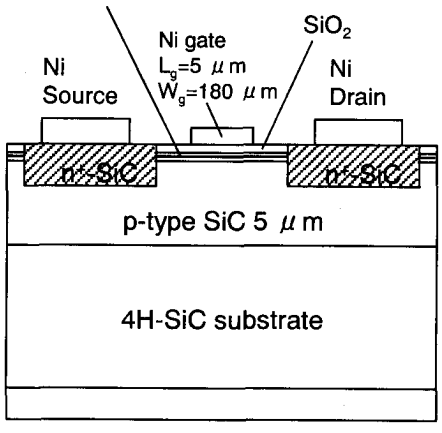

Fig.2. Schematic cross section of the delta-doped accumulation-channel MOS-FET.

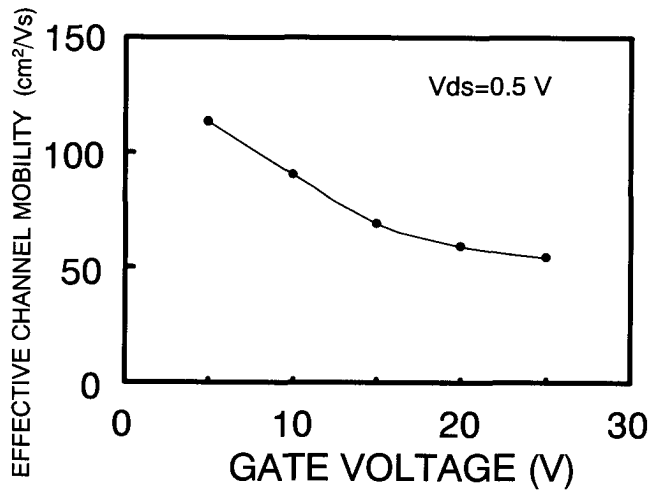

Fig.3. Effective channel mobility vs gate voltage.

5.0kV 4H-SiC SEMOSFET with low RonS of 88 m Ω cm^2

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SiC is expected to enable the realization of power semiconductor devices with better performance than Si devices, because of its superior electrical and physical properties. However, since the built-in junction potential of SiC is higher than that of Si due to its larger band gap, unipolar devices such as FETs and SITs are more suitable than bipolar devices for very low loss, high speed and high voltage applications. Recently, several SiC FETs with better performance than the theoretical limit of Si FETs have been developed [1-3], but their blocking voltages (BVs) are less than 1,800V. For the electric power utility applications, higher BV is needed therefore we have developed 4.5kV SIAFET [4]. In spite of the conductivity modulation in its channel region, its RonS is a relatively high 387 m Ω cm^2 primarily because of poor channel mobility obtained. Recently, we have developed the SEFET (Static channel Expansion FET) device concept and have fabricated 5.5 kV SEJFET with RonS of 130 m Ω cm^2 [5]. In this paper, we report the development of 4H-SiC SEMOSFET (Static channel Expansion MOSFET) with a high performance by an improvement of channel mobility and by an optimization of a device structure. The developed SEMOSFET has high BV of 5020V, low RonS of 88 m Ω cm^2 and high switching speed of about 40ns at the same time. In all reported FETs, the SEMOSFET has the best trade-off between RonS and BV, which exceeds the theoretical limit of 6H-SiC FET for the first time.

Fig.1 shows a cross-sectional structure of SEMOSFET. It has two gates, an accumulated MOS gate, Gm, and a p+ buried gate, Gp, which can electro-statically expand the channel by applying a positive bias and can reduce the channel resistance drastically. Fig.2 is a photograph of the developed SEMOSFET, with a 1.1 mm x 1.1 mm chip size. Fig.3 shows its reverse V-I characteristics. Its BV is 5.02kV and the leakage current density at 4.5kV is 3 x10^{-5} A/cm^2. Fig.4 shows its forward output characteristics. When applied voltages to Gp and Gm are 2.0V and 20V respectively, Ids is 22.8A/ cm^2 at Vds of 2V, therefore, RonS is 88 m Ω cm^2 Fig.5 shows its turn-off waveforms. Turn-off time is 31ns. Turn-on time has also been measured and is 39ns. Fig.6 shows the trade-off between RonS and BV of normally off type FETs reported. The developed SEMOSFET has the best trade-off and exceeds the theoretical trade-off limit of 6H-SiC. Its figure of merit, BV^2/ RonS, is 287MW / cm^2 and is the largest among the reported FETs. The RonS of 5.0kV SEMOSFET is about 1/140th that of the theoretical limit of a Si MOSFET for this BV.

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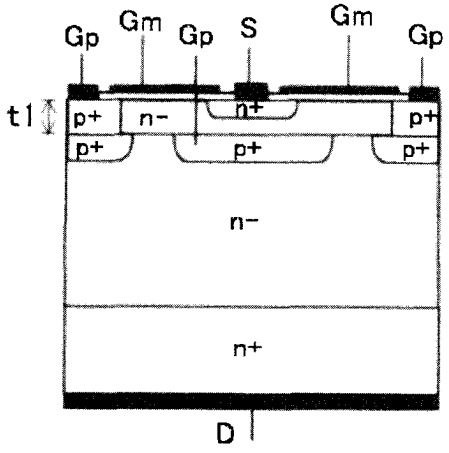

Fig.1. Cross-sectional structure of SEMOSFET.

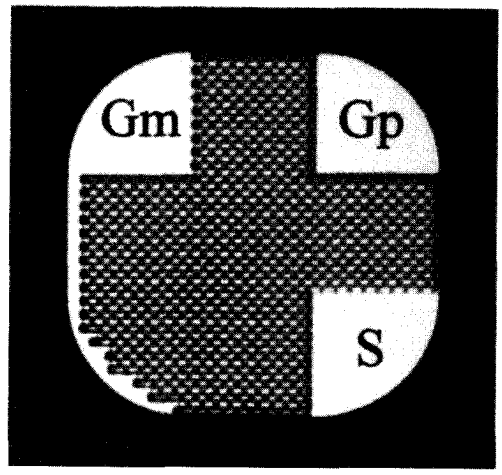

Fig.2. Photograph of developed SEMOSFET.

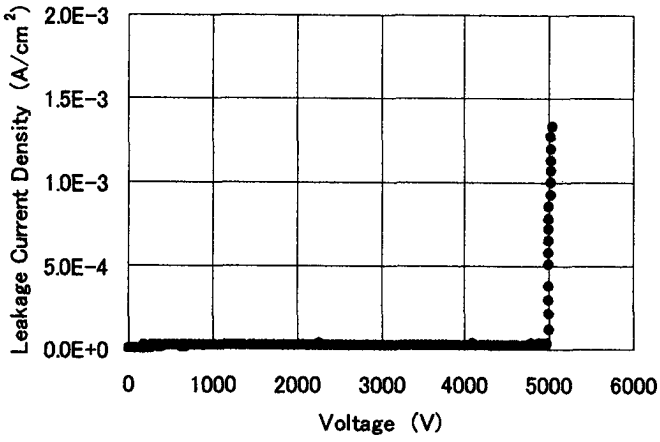

Fig.3. Reverse V-I characteristics.

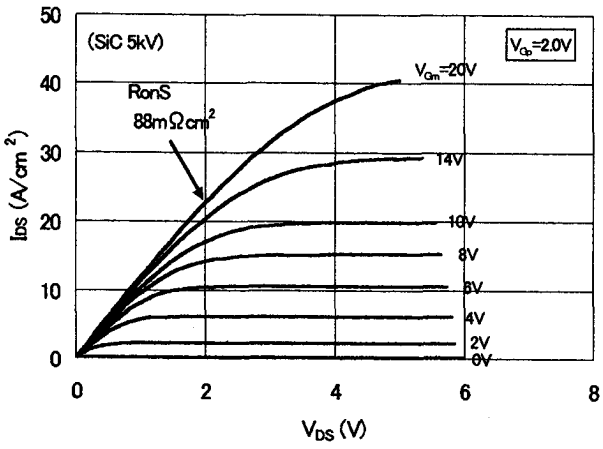

Fig.4. Forward output characteristics.

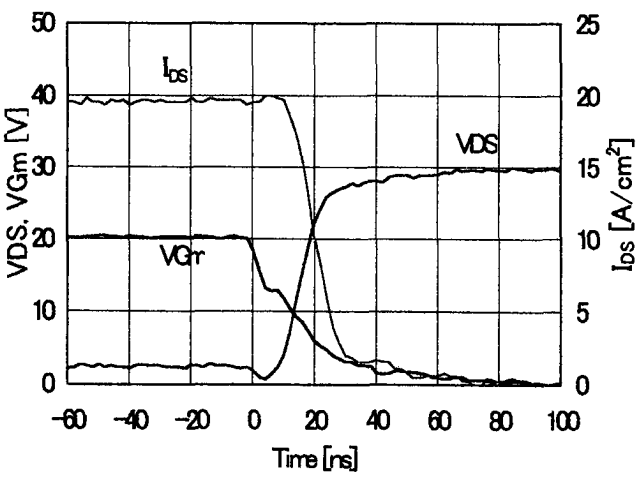

Fig.5. Turn-off waveforms.

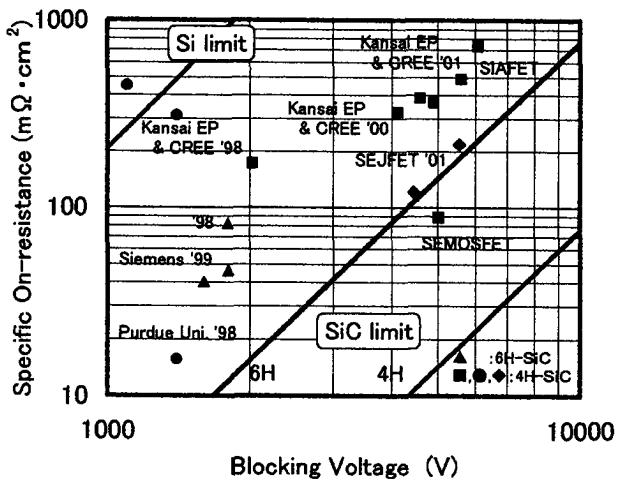

Fig.6. Trade-off between RonS and BV of normally off type FETs reported.

High Performance UMOSFETs on 4H-SiC

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As SiC power switching devices move toward higher operating voltages, it is imperative that proper field terminations be incorporated into the design. Without such terminations, two-dimensional field crowding can occur both internally and at the edges, reducing the breakdown voltage well below that of the theoretical plane junction.

4H-SiC UMOSFETs having both gate trench protection [1] and JTE edge terminations [2] are reported for the first time. The basic device structure is shown in Fig. 1. Two versions of this device are investigated. One version has a thin n-type epilayer grown on the trench sidewalls following RIE to counter-dope the channel, while the other version lacks this feature. Both designs are optimized by extensive 2-D numerical simulations.

In both versions of the device, the gate trenches are protected by an Al implant of $4x10^{13}$ cm^{-2}, 800 nm deep, and the device edges are protected by a 50 μm JTE ring created by implanting Al to a dose of $1x10^{13}cm^{-2}$ and depth of 500 nm. Both implants are annealed at 1550 °C for 30 min. in Ar. A 275 nm gate oxide is formed by thermal oxidation of deposited polysilicon, and a 550 nm polysilicon gate is deposited by LPCVD and doped with phosphorus using spin-on dopant. Ni is used for source and drain ohmic contacts and Al for base and gate trench contacts. All contacts are annealed in Ar at 1000°C for 2 min. The minimum lateral feature size is a conservative 5 μm.

On-state characteristics of both devices are shown in Figs. 2 and 3, and the blocking characteristics in Fig. 4. Because of the thick gate oxide, the threshold voltage is ~ 30 V for the doped-channel FET and ~55 V for the standard FET. The gate voltage is kept below 100 V (oxide field below 4 MV/cm), thereby insuring the long term reliability of the oxide [3]. The doped-channel FET blocks 3,360 V with a specific on-resistance of 199 $m\Omega\text{-}cm^2$ ($V_B^2/R_{ON,SP}$ = 57 MW/cm^2), while the standard FET blocks 3,055 V with a specific on-resistance of 121 $m\Omega\text{-}cm^2$ ($V_B^2/R_{ON,SP}$ of 77 MW/cm^2). To our knowledge, these blocking voltages are the highest reported to date for UMOSFETs in SiC, and the $V_B^2/R_{ON,SP}$ values are close to the highest achieved to date, as shown in Fig. 5. More aggressive layout using 2 μm design rules could easily double this figure of merit.

This work is supported by ONR under MURI grant No. N00014-95-1-1302.

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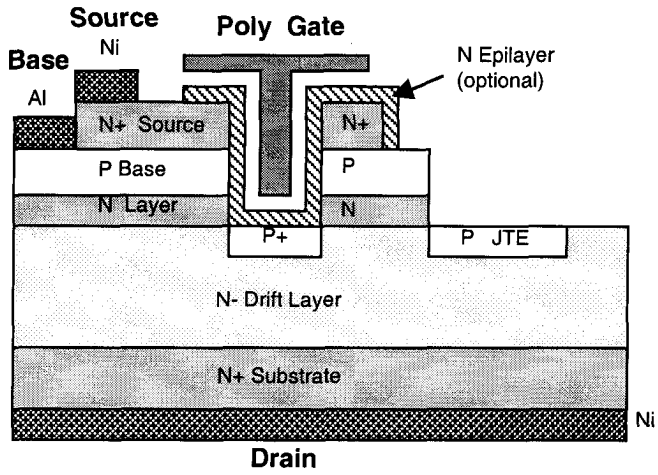

N+ Source:	1e19 cm^{-3} 0.5 μm
P Base:	2e17 cm^{-3} 1.0 μm
N Layer:	2e17 cm^{-3} 0.4 μm
N- Drift Layer:	8e14 cm^{-3} 50 μm
N+ Substrate:	21 mΩ-cm 410 μm
N Epilayer(opt.):	2e17 cm^{-3} 0.1 μm
Gate Oxide:	275 nm
Poly Gate:	550 nm
P+ Trench Impl.:	4e13 cm^{-2} 0.8 μm
P JTE Implant:	1e13 cm^{-2} 0.5 μm

Fig. 1. Structure of the UMOSFET, including JTE edge termination. The JTE is floating, while the gate trench is grounded. The optional N epilayer is present in the doped-channel FET only.

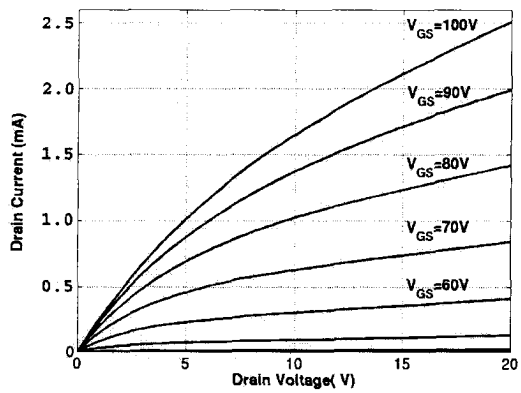

Fig. 2. On-state characteristics of the doped-channel FET. $R_{ON,SP}$ = 199 mΩ-cm^2.

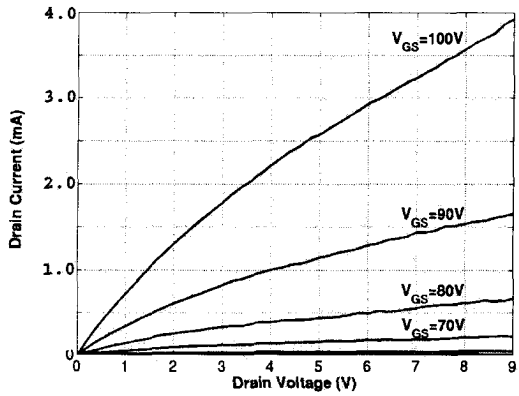

Fig. 3. On-state characteristics of the standard FET. $R_{ON,SP}$ = 121 mΩ-cm^2.

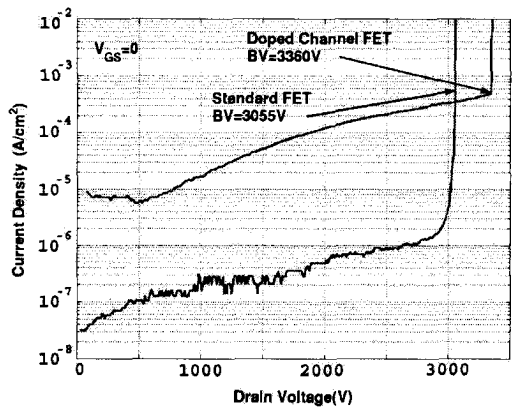

Fig. 4. Blocking characteristics of the doped-channel FET and standard FET.

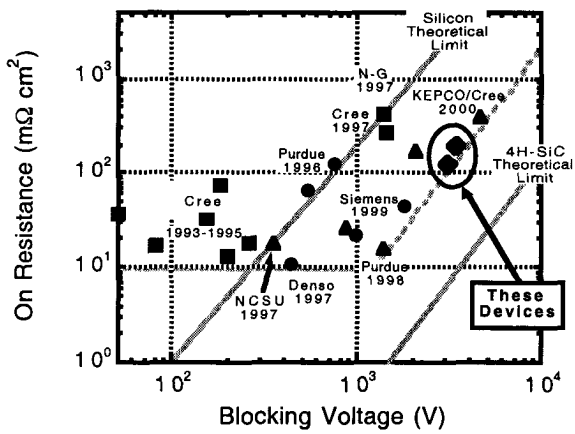

Fig. 5. Performance of recently reported SiC MOSFETs.

SiC Vertical DACFET (Vertical Delta-doped Accumulation Channel MOSFET)

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SiC is a promising material for low loss power device because of its high electric breakdown field and high thermal conductivity. However the low channel mobility of SiC MOSFET is a serious problem to be solved, because the low channel mobility leads to an increase of on resistance directly. Therefore much efforts have been made to increase the channel mobility. We have reported the novel SiC MESFET[1] with delta-doped layered channel and its enhanced channel mobility. Here, we fabricated SiC vertical DACFET that is double implanted MOSFET (DIMOSFET) with delta-doped layered channel and characterized.

The cross sectional structure of vertical DACFET is shown in Fig.1. The Delta-doped layered structure is applied as the channel of conventional DIMOSFET. A10 μm thick n^- epitaxial layer were grown on the low resistive n-type 4H SiC substrate(ρ =0.031 $\Omega \cdot$cm). P-well area was formed by aluminum implantation at 500℃ followed by RIE to remove surface unimplanted region and 1700℃ activation anneal. The carrier concentration of P-well was $1x10^{17}cm^{-3}$ and the junction depth was 1.5 μm from the surface. After the annealing the delta-doped layers were grown on the surface by the CVD system with pulse doping method[2]. The delta-doped layered structure consisted of 10nm thick delta-doped layers ($Nd=1x10^{18}cm^{-3}$) separated by 40nm thick undoped layers. The number of delta-doped layers was four. Source area was formed by nitrogen implantation at 500℃ followed by 1500℃ activation anneal. The gate oxidation was performed at 1100℃ for 3 hours in wet oxygen gas followed by re-oxidation at 800℃ for 2 hours in dry oxygen gas. The gate oxide thickness was around 40nm. Ni was deposited as source contact metal and also as back side drain ohmic contact followed by 1000℃ 5min. rapid thermal annealing (RTA). Al was deposited and patterned as gate electrode. The 500nm thick Silicon-oxide film was deposited with plasma CVD as inter level dielectric. The contact hole was made by RIE and Al was deposited and patterned as upper level metal. The gate length Lg is 10 μm and the spacing S between P-wells is 10 μm.

The typical DC current-voltage (I-V) characteristic of the FET is shown in Fig.2. The chip has 9 square cells. The total gate width and the active area of this device were 2.1mm and $7.0x10^{-4}cm^2$, respectively. Specific on resistance calculated from this active area was 110m$\Omega \cdot cm^2$ at a Vgs of 12V (S=10 μm).

References

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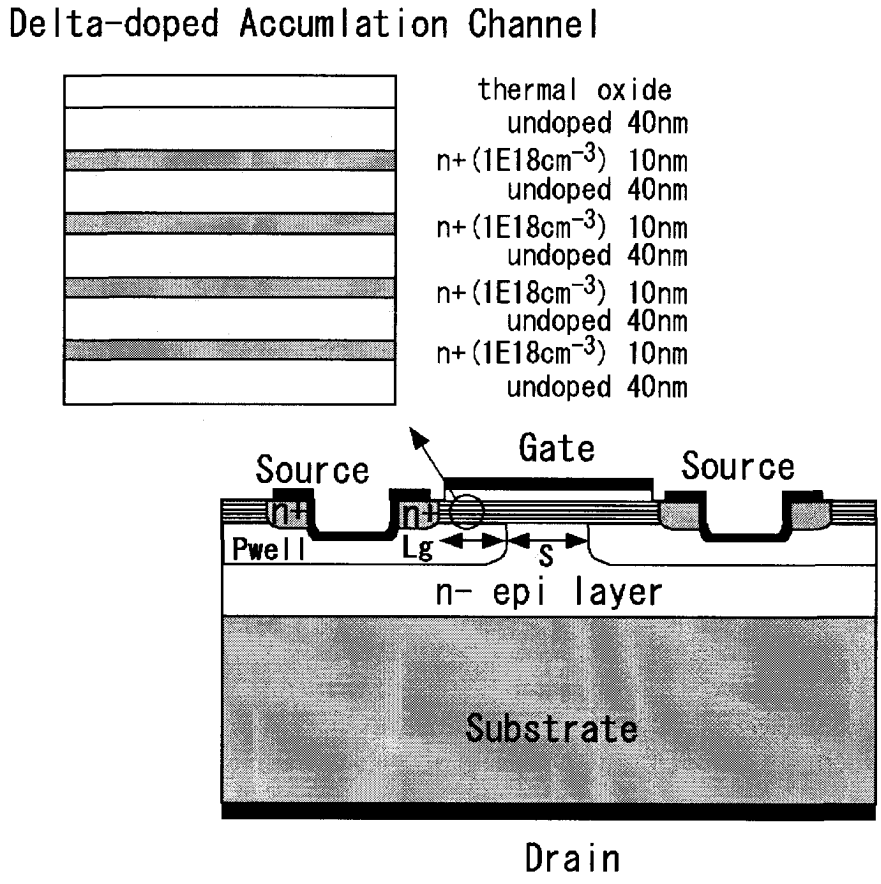

Fig.1 The cross section of SiC DACFET. Left above is the detail of delta-doped layered structure.

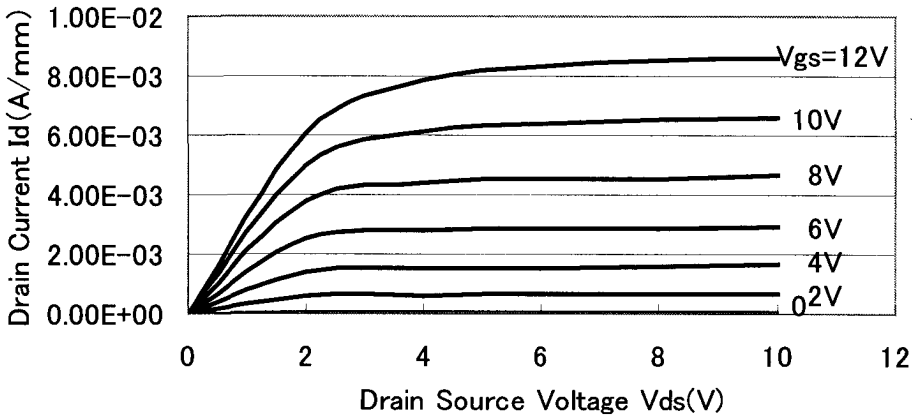

Fig.2 The typical I-V characteristic of SiC DACFET(Lg=10 μ m,W=2.1mm)

Silicon/Oxide/Silicon Carbide (SOSiC) – a new approach for high voltage, high frequencies integrated circuits

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Abstract

A novel device structure/technique termed SOSiC (Silicon On Silicon Carbide) is proposed here for the first time for use in Power Integrated Circuits (PICs). The new device structure is based on Silicon-on-Insulator technology with a SiC substrate in place of a conventional Si substrate. We demonstrate that the change to SiC substrate offers unique and major advantages for high voltage integrated circuits such as (i) significantly increased breakdown voltage due to extension of the depletion region in the SiC substrate, (ii) considerably reduced self-heating owing to the SiC higher thermal conductivity and (iii) higher switching frequency due to the reduced parasitic substrate capacitance. We demonstrate the crucial advantages of this structure in typical high voltage lateral devices through extensive numerical simulations.

SOI in high voltage power integrated circuits

SOI technology is every day winning more and more ground in Integrated Circuits. In particular in PICs, SOI offers a high level of isolation, reduced cross-talk and significantly reduced leakage current compared to standard Junction-Isolation technology. However, the SOI technology suffers from three main drawbacks: reduced breakdown voltage, overheating and lower switching frequency for unipolar devices. The first limits the applicability of the SOI technology to high voltage ICs and imposes a severe limit on the minimum buried oxide thickness. Typically, a thickness of 1-1.5 microns of the buried oxide is needed per 100 V blocking voltage. The higher the thickness of the buried oxide, the stronger the thermal barrier from the active structure to the heat sink leading to severe self-heating. Finally, the switching frequency of LDMOSFETs is lower than that of the Junction-Isolation high voltage ICs due to the absence of the substrate depletion region which serves to decrease the parasitic substrate capacitance during high voltage switching. The absence of the depletion layer in the Si substrate (indifferent of the doping of the substrate) is due to the field plate shield formed by the inversion/accumulation layer which appears under the buried oxide at high voltages.

SOSiC versus SOI

In this paper we propose a completely novel approach to high voltage PICs using a Si/oxide/SiC structure (Fig. 1). In the top Si layer, the active high voltage structures, compatible with CMOS or BiCMOS IC technology are formed. The SiC substrate serves to increase the device breakdown and frequency and, at the same time, reduce self–heating. The buried oxide acts as an electrical isolation layer between the active structures and the SiC substrate. The increase in the breakdown voltage on one hand, and reduction in the substrate capacitance which relates to higher switching frequency on the other hand, rely on the formation of a wide depletion region in the SiC substrate under the buried oxide. This is entirely different from conventional SOI using standard Si substrates. The reason for the depletion region is due to the wide-band gap of SiC substrate. Thus, the charge in the inversion/accumulation surface layer in the SiC substrate is very weak and the charge compensation across the buried oxide is mainly achieved through the formation of a depletion layer in the SiC substrate. Fig. 2 shows the breakdown characteristics for two identical PIN diodes in SOI and SOSiC configurations. The potential distributions at breakdown for a classical SOI and SOSiC structure are shown in Fig. 3 and 4 respectively. As seen in Fig. 4, the potential lines extend deeply into the depletion region of the SiC substrate thus resulting in a more efficient Resurf effect and hence significantly increased breakdown voltage (Fig. 2). Fig. 5 shows, as expected, that owing to the higher thermal conductivity of the SiC substrate, the SOSiC LDMOSFET is also less prone to self-heating than its conventional SOI variant. Finally, as already mentioned, the formation of the depletion region in the SiC substrate in the SOSiC LDMOSFET leads to a reduction in the drain/substrate capacitance, which in turn results in a faster switching. This is proven by looking at the inductive switching of an LDMOSFET in SOSiC compared to a conventional SOI in identical inductive conditions (Fig. 6).

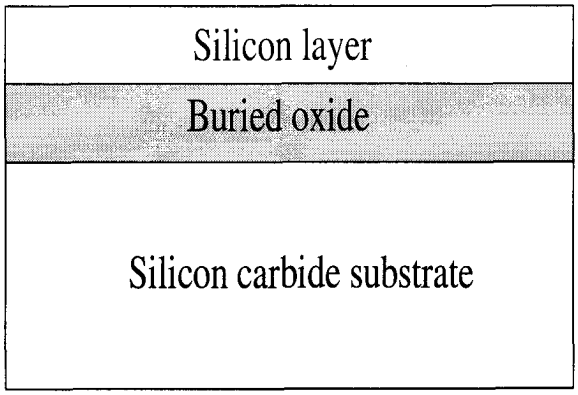

Fig. 1 Schematic cross section of the silicon/oxide/silicon carbide (SOSiC) structure

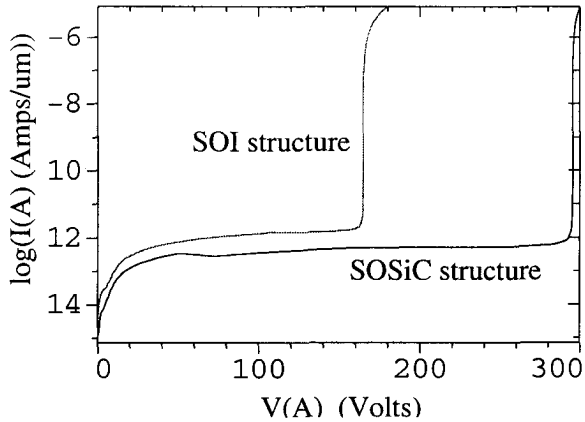

Fig. 2 The breakdown characteristics for two identical PIN diodes in SOI and SOSiC configurations

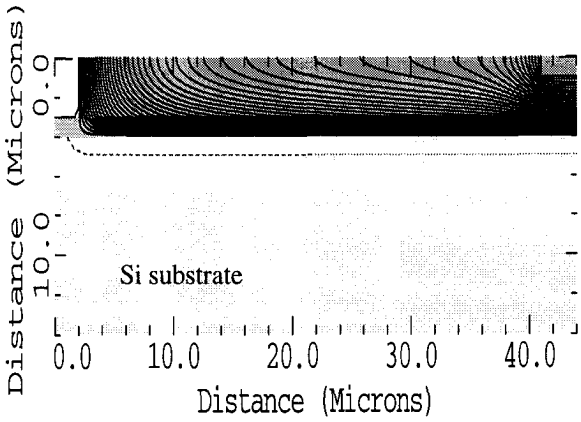

Fig. 3 The potential distribution at breakdown for a classical SOI PiN diode – V_{BR}=168V

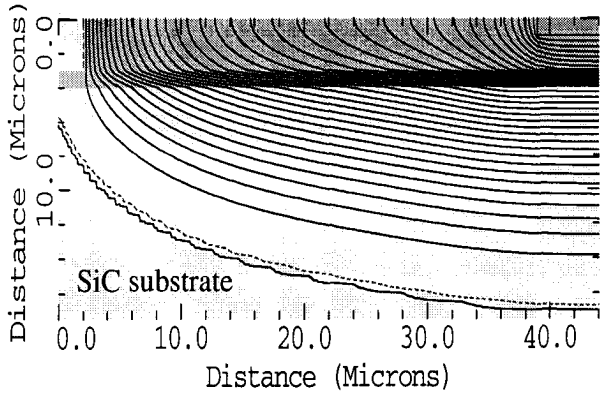

Fig. 4 The potential distribution at breakdown for a SOSiC PiN diode – V_{BR}=299V

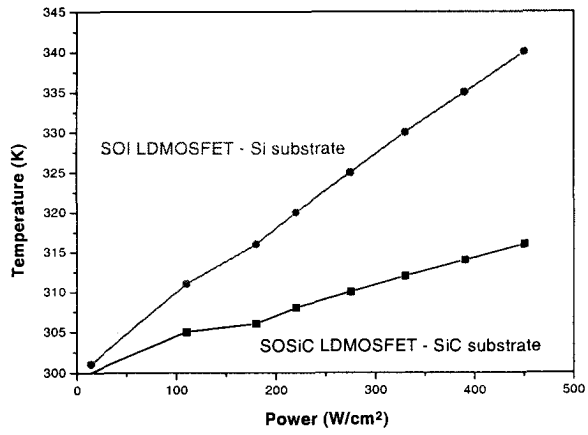

Fig. 5 The self heating effect represented in a conventional SOI LDMOSFET and in a novel SOSiC structure LDMOSFET.

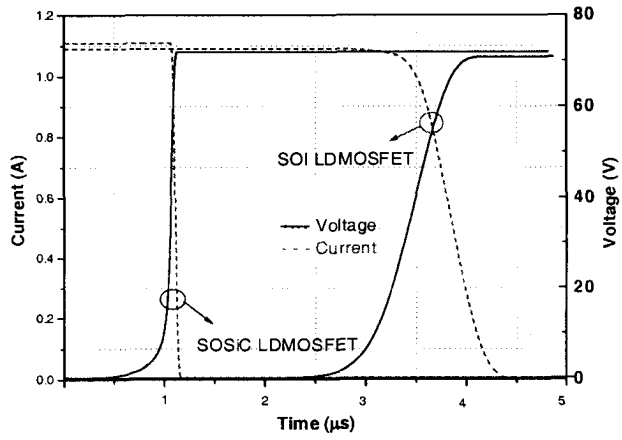

Fig. 6 The inductive switching behaviour of a conventional SOI LDMOSFET and a SOSiC LDMOSFET